National Semiconductor

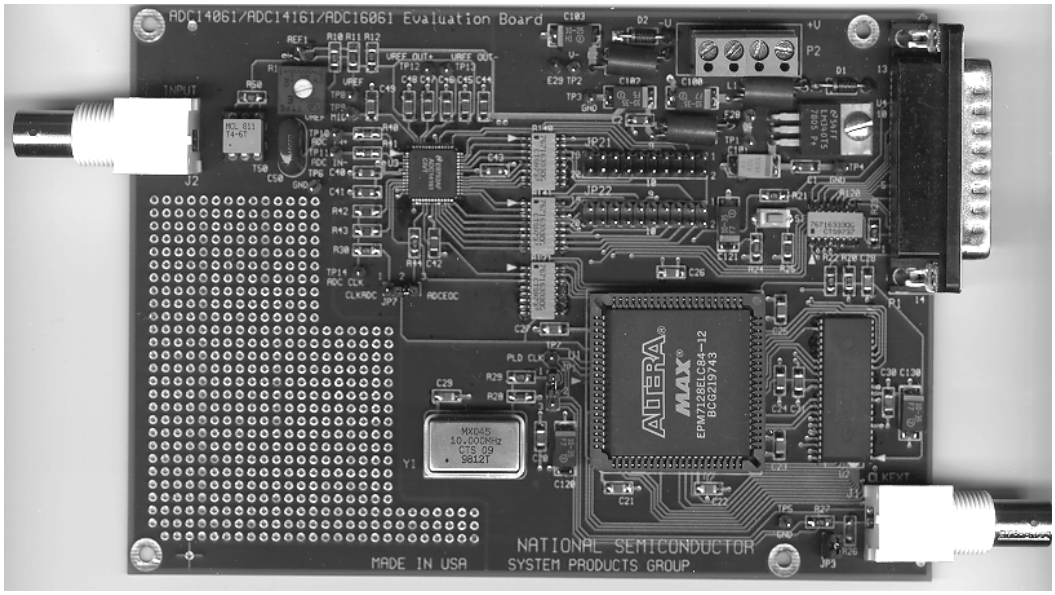
April 2004
Rev 4

Evaluation Board Instruction Manual

ADC14061 / ADC14161 (Lifetime Buy issued)
14-Bit, 2.5 MSPS, 390mW Analog-to-Digital Converters

and

ADC16061
16-Bit, 2.5 MSPS, 390mW Analog-to-Digital Converter



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1.0 Introduction

The ADC14061EVAL Design Kit (consisting of the ADC14061 Evaluation Board, National's WaveVision™ software and this manual) is designed to ease evaluation and design-in of National's ADC14061, ADC14161 and ADC16061 14-bit and 16-bit, 2.5MSPS Analog-to-Digital Converters. Whenever the ADC14061 is mentioned in this manual, the ADC14161 and the ADC16061 are also included.

The WaveVision™ software can be operated under Microsoft Windows 3.1 or later, but will NOT work with Windows NT. The signal at the Analog Input is digitized and can be captured and displayed on the computer monitor as dynamic waveforms. The digitized output is also available at a pair of headers: JP21 and JP22.

The software can perform an FFT on the captured data upon command. The FFT display also shows dynamic performance in the form of SNR, SINAD, THD and SFDR data.

While a socketed transformer is present on an assembled board, a large prototype area is available for building customized input conditioning circuitry.

2.0 Quick Start

1. Unless the ADC14061 Evaluation Board has been pre-assembled, it needs to be assembled before operation. Refer to Figure 1 for the location of major components on the board. Refer to section 9.0 for the bill of materials.
2. Construct the desired input conditioning circuitry.
3. Connect the interconnecting cable from connector P1 to an available parallel port on your PC. Be sure the interconnecting cable is a 1 to 1 cable with all pins wired.
4. Connect a voltage source (+8V to +12V) and ground to Power Connector P2.
5. Adjust R13 for 2.0V at E8. This sets the ADC14061 reference voltage.
6. Connect a 50 Ohm signal generator to BNC J2 and adjust its output for a signal excursion between the limits of 1V and 3V. **Be careful not to overdrive the ADC14061 input.**
7. Copy the WaveVision™ software (ADC14061.EXE) to the desired computer hard drive directory and run it.
8. Press the Reset button (S1) on the board.
9. Select the parallel port (under the Options menu) that is to be used.
10. Capture data by pressing CTRL-X.
11. Perform an FFT on the data that was acquired by pressing CTRL-F.

3.0 Functional Description

Figures 8 and 9 show the block diagram of the ADC14061 evaluation board. U10 is the ADC under test. This board supports the ADC14061, the ADC14161 and the ADC16061 converters.

3.1 Input signal conditioning.

The board contains a breadboard area to be used as needed. The input signal to be digitized should be applied to BNC connector J2. If the input signal may contain information at frequencies greater than ½ the clock frequency, you should include an appropriate anti-aliasing filter in the input circuitry.

Note that the input signal to the ADC14061 should not swing below 1V, or go above 3V, assuming a 2.0Volt reference and 2 Volt V_{CM}. If the input signal to the board goes outside of either of these limits, you should include an appropriate offset in the conditioning circuitry.

3.2 ADC reference circuitry.

The ADC14061 operates with a nominal reference voltage of 2.0V. The acceptable reference voltage range is

$$1.8V \leq V_{REF} \leq 2.2V.$$

This board, if assembled, comes with a LM4041-ADJ adjustable reference.

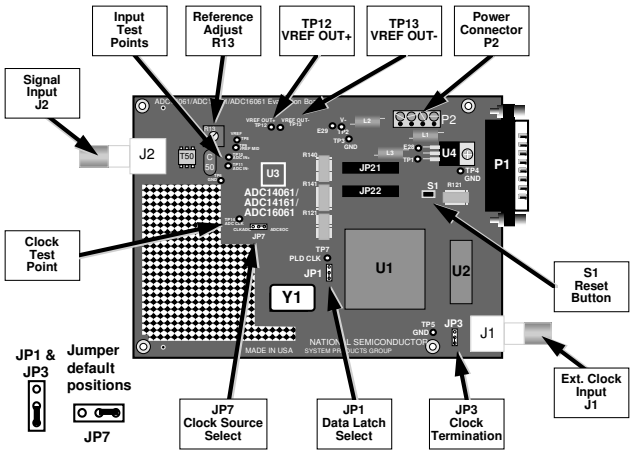


Figure 1. Component and Test Point Locations

3.3 Board Outputs.
The buffered digital data from the ADC14061 output, as well as a clock signal for this data, is available at 20 pin headers JP21 and JP22. These connectors have all the even numbered pins grounded and is suitable for connecting ribbon cables to the board.

JP7 is used to select whether the ADC clock or the EOC signal from the ADC is used to clock the data. The default is to use the ADC EOC signal to clock the data.

3.4 Board Control.
PLD U1 is a state machine that performs the control functions of the board. It also contains registers and logic used to move data. The functions of this device are:

- Write acquired data to RAM.
- Accept commands over the computer.
- Upload data in RAM to PC via parallel port link upon command.

3.5 Data Memory.
The data memory consists of a single 64k x 16 RAM chip, U2. Data is written to RAM from the ADC14061 via PLD U1. During data acquisition, the RAM address is incremented by U1. Data is read from RAM by U1 and sent over the computer-board cable. The number of words sent is determined by the instructions from the host computer.

3.6 Computer Interface.
The board communicates with a host computer through a parallel interface. The data path is through the DB-25 connector P1, located at the right side of the board. The parallel interface uses a PC parallel port that must support EPP or ECP modes.

3.7 Power requirements.
Power is supplied to this board through power connector P2 at the top right of the board. The board requires 100mA at +8V to +12V. There is a connection for a negative supply, should you need it for any input conditioning circuitry. The board is protected from accidental polarity reversal through the use of series diodes in both the positive and negative voltage lines.

4.0 Installing the ADC14061 Evaluation Board and WaveVision™ Software

The evaluation board requires power as described in paragraph 3.7. No input signals for evaluation are generated on the board. An appropriate signal generator (such as HP8662A) with a 50- to 75-Ohm source impedance should be used to evaluate the performance of the ADC14061. The generator output should be filtered by a bandpass filter to eliminate unwanted frequencies from the generator. This will provide dynamic readings that are a more accurate assessment of the converter performance than you would obtain without the filter.

4.1 Software Installation
The WaveVision™ software provided requires 350kb of hard drive space and will run under Windows 3.1 or later, but NOT Windows NT.

1. Insert the disk into a 3.5" floppy drive.
2. Copy the program ADC14061.EXE to the desired subdirectory on you computer's hard disk.
3. From file manager, select the program ADC14061.EXE and RUN it.

You may create a new directory and/or program group with icon to allow easy program execution by following the steps below.

4.1.1 Creating a New Directory
To create a new directory, follow these steps:

- Open the File Manager and click on any folder.
- Press the HOME key to go to the root directory.
- Select File/Create Directory
- Enter the name of the directory you desire to create, such as ADC14061, and click on "OK".

4.1.2 Adding a Program Group and Icon
If you desire to add a Program Group and Icon to the Program Manager, you may do so by following the instructions below.

4.1.2.1 Adding a Program Group

- From the Program Manager, select File, New.
- Select Program Group and click OK
- Enter an appropriate Description, such as "ADC14061 Evaluation" and click OK.

4.1.2.2 Adding an Icon to a Program Group

- From the Program Manager, select File, New.
- Select Program Item and click OK
- Enter an appropriate Description, such as "ADC14061", and click Browse.
- Find and double click on the directory where you loaded the program ADC14061.EXE.
- Select the program ADC14061.EXE and click OK.
- Click on Change Icon.
- Select the Icon and click OK.
- Click OK again.

4.2 Installing the ADC14061 Evaluation Board

The procedures given here will help you to properly set up the board, although it was designed to be easy and simple to use.

4.2.1 Board Set-up

Refer to Figure 1 for locations of connectors, test points and jumpers on the board.

1. Connect power to the board per paragraph 3.7.
2. Connect a cable with DB-25 connector between parallel port connector P1 and a parallel port on your computer.
3. Be sure a 10MHz clock oscillator (U1)is in place, or connect an external clock source to BNC J1 at the lower right corner of the board.
4. Be sure jumper JP1 is set to select the clock source used.
5. If using an external clock source, place a shorting bar across the pins of JP3 to terminate the clock input.
6. Connect an appropriate signal source to J2.

4.2.2 Quick Check of Analog Functions

Refer to Figure 1 for locations of connectors, test points and jumpers on the board. If at any point the expected response is not obtained, see section 4.2.4 on Troubleshooting.

1. Perform steps 1 through 6 of Section 4.2.1.
2. JP1 - Short upper two pins to select the on-board clock oscillator.
3. JP7 - Short left two pins to use the ADC clock to clock data into RAM.
4. Turn on the power to the board.
5. Adjust R13 for a voltage of 2.0V at TP8.
6. Connect a signal source to Analog Input BNC J2. Signal amplitude should be approximately $2V_{P-P}$, centered around 2V.
7. Scope the signal at TP10 to be sure that it is present and does not go below 1.0V or above 3.0V.

This completes the testing of the analog portion of the evaluation board.

4.2.3 Quick Check of Software and Computer Interface Operation

1. Perform steps 1 through 6 of Paragraph 4.2.2, above.
2. Disconnect any signal from J2, ADC14061 analog input.
3. Be sure there is an interconnecting cable between the board and your computer parallel port.
4. Run program ADC14061.EXE.
5. Acquire data by clicking on the ACQUIRE icon or by typing ALT, P, X or CTRL-X. The status bar at the bottom of the window should indicate Receiving Data. Data transfer can take a few seconds.
6. When transfer is complete, the data window should show a horizontal line at approximately the 0 (zero) code level.
7. Supply a 1Vp-p sine wave of 100kHz to 500kHz at Analog Input BNC J2.
8. Repeat step 5, above.
9. When transfer is complete, the data window should show many sine waves. The display may show a nearly solid area of red, as in Figure 2, which is O.K.

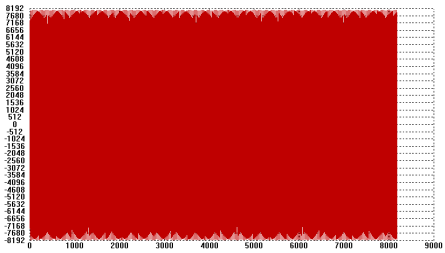


Figure 2. The WaveVision™ captured display of a 400kHz sine wave at 2.5MSPS. The input signal should be filtered to remove harmonic distortion and should be stable to prevent averaging of the data in the FFT process.

10. With the mouse, click and drag to select a small portion of the displayed waveform.
11. Adjust the input at J2 to ensure that the waveform does not reach codes of 8191 or -8192. Optimum performance measurements occur when the lowest and highest codes digitized are near but not at the limits of 8191 or -8192. Try to get to within 100 codes of both extremes.

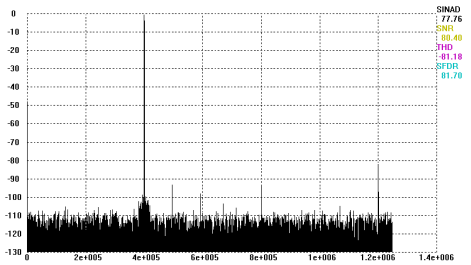


Figure 3. FFT display of the signal in Figure 2 showing performance of the ADC14061. From this display, the noise floor can be measured and spurious signals can be identified. Note the display of SINAD, SNR, THD and SFDR to the right of the plot.

12. Repeat steps 8 through 11 above until the signal is centered and extends on the low end to a code between -8100 and -8190 and extends on the high end to a code between 8100 and 8190.
13. Click on the FFT icon or type ALT, P, F or CTRL-F.

The FFT data will provide a measurement of SINAD, SNR, THD and SFDR (See Figure 3), easing the performance verification of the ADC14061.

4.2.4 Troubleshooting

"Error Transmitting", "Parallel Port Time Out Error" and/or "Failed to communicate with the board on LPT1" errors mean communication was unsuccessful. Try the following:

- Reset the evaluation board by pressing button S1 and try again.
- Be sure that the ADC14061 board is connected and has power.
- Be sure cable connections are solid.
- Be sure the correct parallel port is selected.
- Be sure that the parallel port jumper or BIOS settings are set to enable bi-directional EPP or ECP modes.

If there is no output from the ADC14061, perform the following:

- Reset the evaluation board by pressing button S1 and try again.
- Be sure proper voltage(s) are at the correct pins of power connector P2.
- Be sure clock signal is present at TP14.
- Check for presence of jumpers on JP1 and on JP7.
- If the displayed waveform appears to be garbage, reset the evaluation board by pressing button S1.

4.3 Jumper Information

Table 1 indicates the function and use of the jumpers on the ADC14061 evaluation board.

JUMPER	FUNCTION	PINS 1 & 2 SHORTED	PINS 2 & 3 SHORTED
JP1	Select Clock Source	Select On-Board Crystal	Select Ext. Clock
JP3	Terminate Ext. Clock	50-Ohm Termination	N/A
JP7	Select Data Latch Signal;	Select ADC Clock	Select ADC EOC

Table 1. Jumper settings.

5.0 Exploring the Waveform

WaveVision™ software and the ADC14061 Evaluation Board add a new tool to the designer's toolbox. The evaluation board can be used to capture a signal. The captured data can then be displayed on a computer monitor and performance parameters can be estimated.

After the ADC14061 Evaluation Board has uploaded a captured waveform to the PC, WaveVision™ displays this waveform on the computer monitor. You should realize that any amplifier used before the ADC14061 can affect the apparent performance of the ADC because most available amplifiers exhibit more distortion than does the ADC14061. The characteristics of any transformer you may use can also affect the overall circuit performance.

See the Appendix for WaveVision™ screen drawings of software operation.

5.1 Signal Purity

Not all sine wave generators can produce a signal pure enough to adequately evaluate a 14-bit ADC. Since the SINAD of a perfect 14 bit ADC is 86dB, any input signal should be at least 6dB better than this, or have a SINAD of 92dB or better! Even some very expensive signal generators can not produce such a clean signal.

To ensure that any input signal is clean, you can insert a low pass filter in series with the input signal. Comparing the dynamic response with and without this filter is an education in itself.

The elliptic filter of Figure 4 is an example of a suitable filter. It has attenuation of about 3dB at 800 kHz, 32dB at 1MHz and 64 dB at 1.5 MHz.

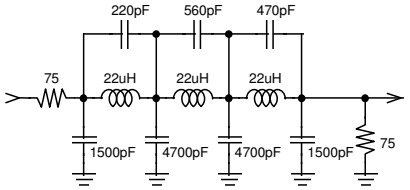


Figure 4. This elliptic filter should be driven by a generator of 50 to 75 Ohms source impedance and terminated with 50 to 75 Ohms. The input resistor shown here is normally included in the generator.

5.1.1 Evaluating a Sine Wave

Set the ADC clock frequency to 2.5MSPS as follows:

1. Be sure that a 10MHz oscillator (U1) is in its socket.
2. Select the Procedures pull-down menu and the Configure Board submenu, or type CTRL P.
3. Be sure that the lower left of the dialog box indicates a 10MHz crystal.
4. Set the clock divide by number to 4 by typing CTRL-P and changing the "Board to ADC Clock Ratio" to 4 (choices are 4 and 8).
5. Click on OK.
6. Connect a signal generator to input BNC J2.
7. Adjust the generator to provide a 5kHz to 6kHz output with minimum and maximum extremes of about 1.1V to 2.9V.
8. Capture the signal (Procedure Execute or CTRL X) and wait for it to be displayed on your monitor.
9. Select a small portion of the waveform by clicking and dragging across it. Do this again, until you have just a few cycles on the screen, then select either a single rising or a single falling slope between the codes of about -4000 to +4000 on the ordinate (vertical) axis.

You can now examine the slope for any non-monotonic behavior or excessively small or large step sizes.

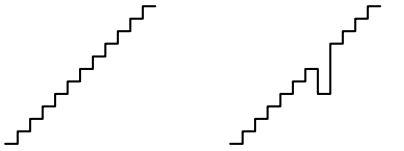
Lower the frequency to a few hundred Hz and repeat the above steps. You will notice that any non-monotonicity will appear worse at lower input frequencies. This is normal because the slow ramp causes the input to remain near switching thresholds for longer periods of time.

5.1.2 Low Frequency Triangle Wave Input

A low frequency (about 1KHz) triangle wave will provide general information on ADC performance.

5.1.2.1 Monotonicity and Uncertainty

When a voltage ramp is digitized, the code sequence shows increasing codes up to the peak level, or decreasing codes to the minimum level, depending upon whether the slope is positive or negative. A monotonic condition is one where the code sequence does not show any reversals, as in Figure 5a.



a. Monotonic Signal b. Non-Monotonic Signal

Figure 5. Monotonicity means codes are continually increasing or decreasing.

A converter that has one or more instances of codes going in the wrong direction is said to be non-monotonic. The resulting reconstructed waveform might be as shown in Figure 5b.

When digitizing signals with rise and fall times slow enough to result in more than one conversion result of the same code in sequence, it is normal to have some code uncertainty when the input is at a code transition point. See Figure 6.

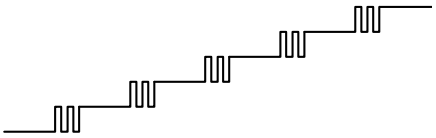


Figure 6. Code uncertainty when the ADC input voltage is near a code transition point.

5.1.2.2 Rising / Falling Symmetry

The ideal analog-to-digital converter will give the same code when digitizing a given input voltage whether that voltage is approached from a lower voltage or from a higher voltage. If a triangle wave is presented to the ADC, the falling side of the waveform should be a mirror image of the rising side at the input and at the output. In practice, however, this may not be the case. Noise anywhere in the system may cause the rising and falling slopes to differ, as can the signal source itself. Looking at the WaveVision™ data display of a digitized triangle wave will show how symmetrical the two slopes are with respect to each other *provided the input signal has symmetrical slopes*. Choose your generator with care as many triangle wave signal generators have non-symmetrical slopes.

5.2 The FFT Plot

The readings of SINAD, SNR, THD and SFDR (Spurious-Free Dynamic Range) are only meaningful for a single frequency sine wave input to the ADC and are only accurate to the extent that the input waveform to the ADC14061 is clean (contains a single frequency) and stable.

5.2.1 Dynamic Performance Estimates

The dynamic performance as indicated by SINAD, SNR, THD and SFDR are estimates rather than hard and fast figures because their accuracy depends upon how much of the ADC14061's dynamic input range is used, and how many samples are taken.

For example, if the input is reduced below a full scale swing such that the maximum and minimum codes obtained at the output are 7500 and -7500, rather than the full scale values of 8192 and -8191, only about 91% of the code range is used. The result is an apparent degradation of SNR. On the other hand, if the input exceeds the input dynamic range such that the top or bottom (or both) of the input signal is clipped at the ADC14061's input, THD, SFDR and SINAD will be degraded.

Furthermore, apparent performance may be limited by the purity of the input signal used, or by the non-linearities of any op-amp or other signal conditioning circuitry.

5.2.2 Bandwidth Estimation

If a constant amplitude frequency sweep is applied at the Analog Input (J2) and the signal at the ADC input is digitized and displayed, the data display on your computer monitor will show any frequency dependent amplitude variation. If you then perform an FFT on this data, you can effectively see the amplitude response in the form of a Bode plot.

6.0 Computer-Board Communications

Communication between the board and computer are through a parallel port connection at connector P1. The board responds to commands from the computer and uploads data requested by the computer.

The RAM address is incremented by PLD U1, which clocks the ADC14061 output data into a latch within U1, then sends it RAM. The PLD (U1) counts the number of words it clocks into RAM. Once the requested number of words has been acquired, the board uploads the data to the host computer.

7.0 Circuit Description and Hardware Schematics

Figure 7 shows the block diagram of the ADC14061 evaluation board. U1 (a programmable logic device) controls I/O and interprets instructions from a host PC that is operating under WaveVision™ control. After receiving a command from the host PC, the evaluation board interprets it, performs the operation requested and returns the results. The board operates from a single supply of +8V to +12V. A connection is provided for a negative supply, should one be needed for any input conditioning circuitry.

The hardware schematic is divided into two sections: The Input, Reference and Test Device Section, and the Control, Memory, Communications and Power Supply Section.

7.1 Input, Reference and Test Device Section

Figure 8 shows the input processing, reference and test device circuitry. The Analog Input at J2 will be presented to the converter via any signal conditioning circuitry that you may build. No anti-aliasing filter is included with the board. You should add such a filter, if needed.

7.2 Control, Memory, Communications and Power Supply Section

The Control, Memory and Power Supply Section is shown in Figure 9. The PLD (U1) is a state machine that controls the functions of the demonstration board.

Output data from the ADC14061 is re-clocked through U2 and stored directly to RAM (U2). The stored data is read from RAM and sent to the host computer by U1.

Power is brought to the board at P2. The supplies are protected with series diodes.

The ADC14061 will operate with clock frequencies of 300kHz to 2.5MHz. U1 will divide the on-board clock oscillator by either 4 or 8, depending upon user command (See Section 5.1.1 and Appendix). Accordingly, the board will function with clock oscillators in the range of 1.2MHz to 20MHz, as long as the ADC14061 clock frequency is in the range of 300kHz to 2.5MHz.

7.3 The Reset Button

The Reset button (S1) is used to reset U1. This button should be pressed after applying power to the board and any time the system does not appear to be working properly.

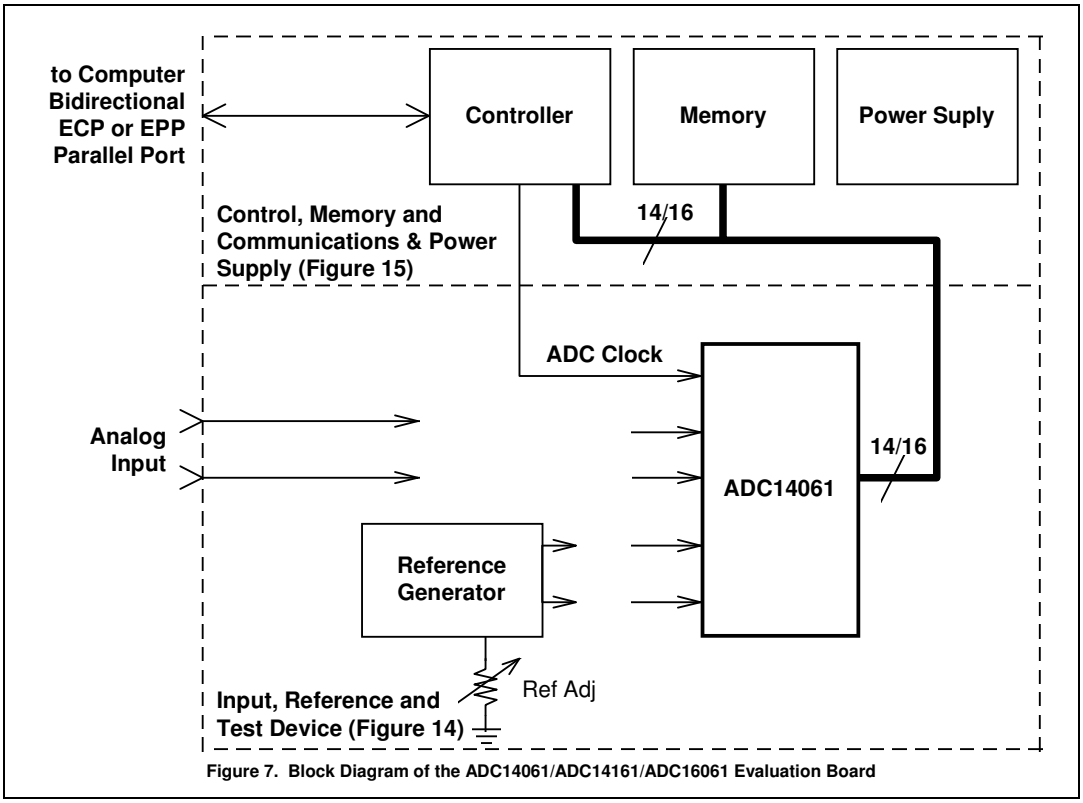


Figure 7. Block Diagram of the ADC14061/ADC14161/ADC16061 Evaluation Board

7.4 Hardware Schematics

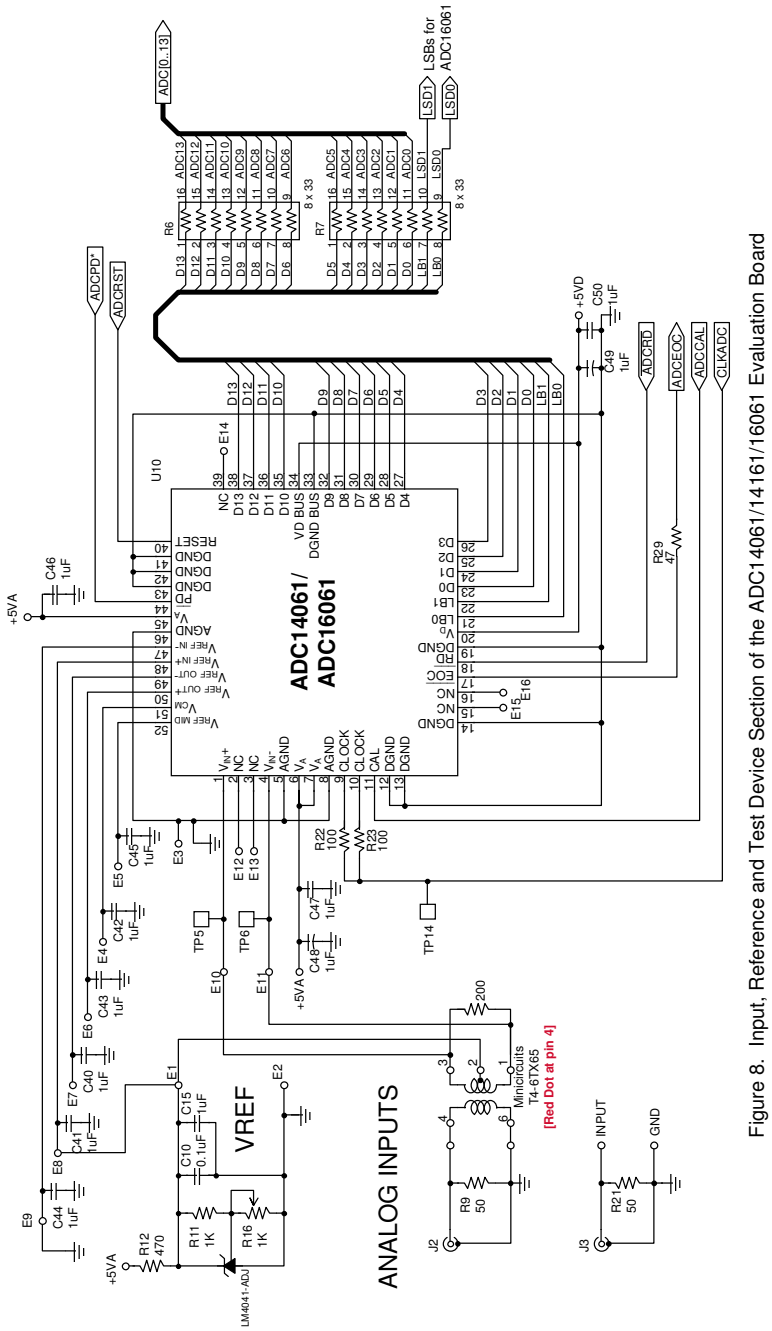


Figure 8. Input, Reference and Test Device Section of the ADC14061/14161/16061 Evaluation Board

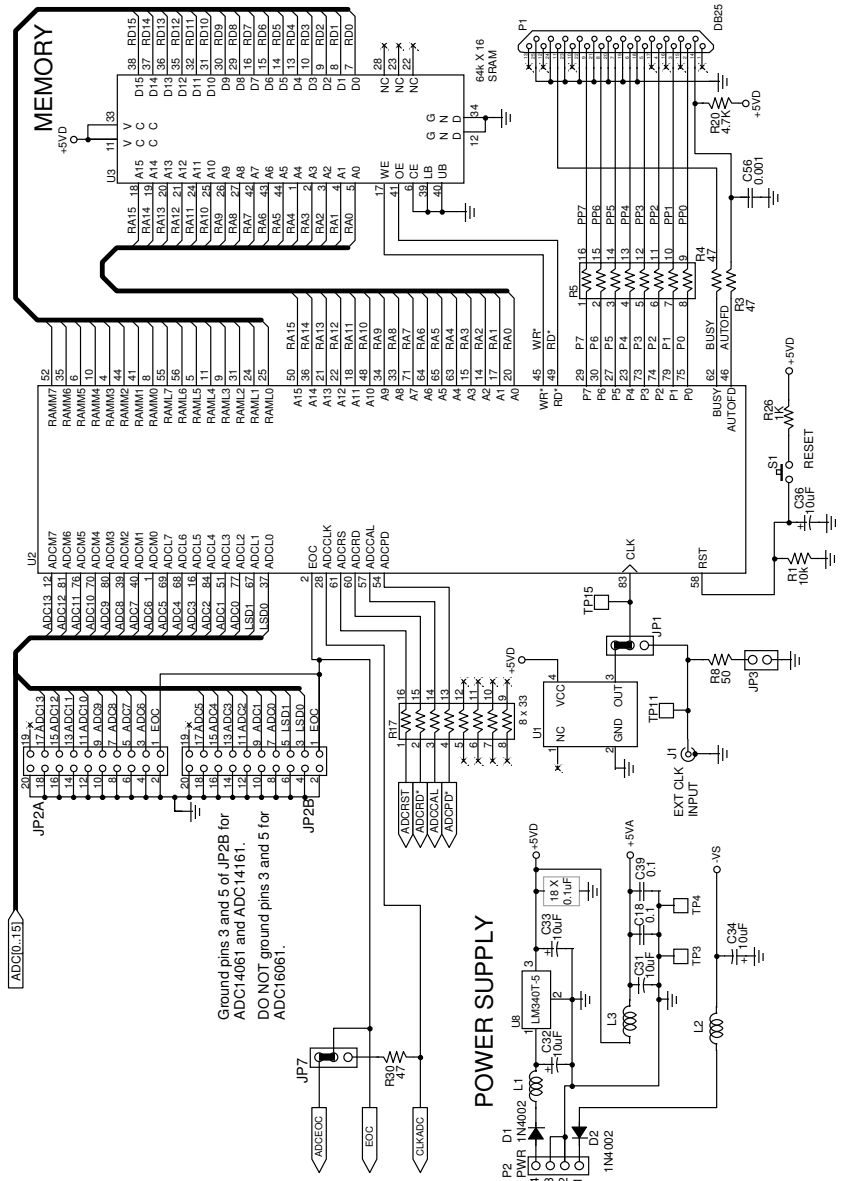


Figure 9. Control, Memory, Communications and Power Supply Section of the ADC14061 Evaluation Board

8.0 Bill of Materials

Designator	Value	Type/Source
C50	220pF	Silver Mica
C28	0.001uF	Type 1206
C20, C21, C22, C23, C24, C25, C26, C27, C29, C30, C31	0.1uF	Type 1206
C1, C2, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49	1uF	Type 1206
C100, C102, C103, C120, C121, C130	100uF, 15V	Type 7343
C101	100uF, 6V	Type 7343
D1, D2	1N4001	Various
J1, J2	BNC	DigiKey # ARF1177-ND
JP3	2-PIN Post Header	DigiKey # A19350-ND
JP1, JP7	3-PIN Post Header	DigiKey # A19351-ND
JP21, JP22	10 x 2 Header	DigiKey # 2011-36-ND
--	Shorting Jumper (3 needed)	DigiKey # S9001-ND
L1, L2, L3	Choke	DigiKey # M2204-ND
P1	DB25 Connector, Male, Right Angle	DigiKey # A2098-ND
P2	Terminal Block	DigiKey # ED1609-ND
R24	10k, 5%	Type 1206
R40, R41	33 Ohm, 5%	Type 1206
R21, R22, R23, R27, R29, R30, R44	47 Ohms, 5%	Type 1206
R26	50 Ohms, 5%	Type 1206
R25, R42, R43	100 Ohms. 5%	Type 1206
R50	200 Ohm, 5%	Type 1206
R10, R12	470 Ohms, 5%	Type 1206
R11, R28	1K, 5%	Type 1206
R20	4.7k, 5%	Type 1206
R120, R121, R140, R141	33-Ohm Resistor Pack	DigiKey # 766-163-R33-ND
R13	1K Potentiometer	DigiKey # 3386F-102-ND
REF1	LM4041DIM3-ADJ	National Semiconductor
S1	Push Button Switch, SPST-N.O.	DigiKey # P807S-ND or CKN9016-ND or CKN9017-ND
TP1 thru TP14	Breakable Header	DigiKey # S1012-36-ND
T50	RF Transformer	Minicircuits T4-6TX65
U1	EPM7128ELC84-15 (w/programming)	Altera
U2	TC551664AJ-15	Toshiba
U3	ADC14061CIVT	National Semiconductor
U4	LM340T-5	National Semiconductor
Y1	10MHz Oscillator	DigiKey # CTX114-ND
-	6-pin Socket for Transformer	DigiKey # AE8906-ND
-	4-Pin full-size oscillator socket	DigiKey # A462-ND

9.0 Saving and Retrieving Files

WaveVision™ allows your to save data in two formats. One is a binary file, the other is an ASCII file.

9.1 Binary Files

A binary file is intended for use only by WaveVision™ and contains information as to program settings as well as the raw waveform data.

To save a binary file for use later by WaveVision™, you can click on the Save icon, enter ALT, F, S or enter CTRL-S. You will be prompted for a file name the first time you save a given set of data.

To save a file that has already been saved, but to save it under a different file tame, enter ALT, F, A. You will be prompted to enter the new file name.

To retrieve a binary file in WaveVision™, you may click on the Open File icon, enter ALT, F, O or enter CTRL-O. You will be prompted for the name of the file you wish to retrieve.

9.1 ASCII Files

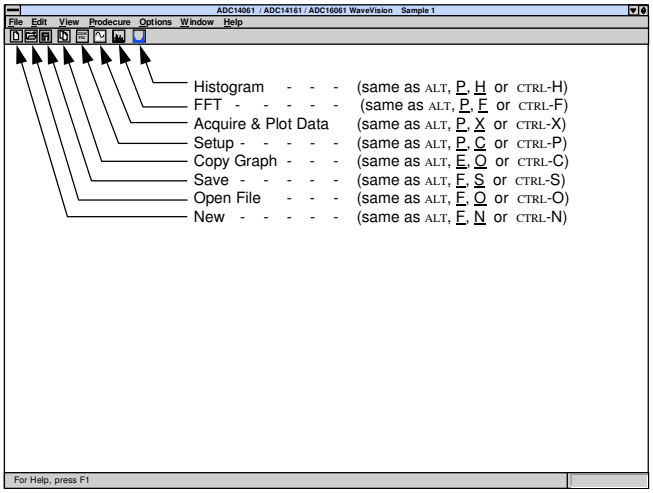
To export (save) an ASCII file for use later by another program, such as a spreadsheet, you must enter ALT, F, D. You will be prompted for a file name. The ASCII file will contain only raw data with one data point per line.

To import (retrieve) an ASCII file, whether created with WaveVision™ or with any other program or utility, enter ALT, F, I. You will be prompted for the name of the file you wish to retrieve. Remember that imported files must have one data point per line.

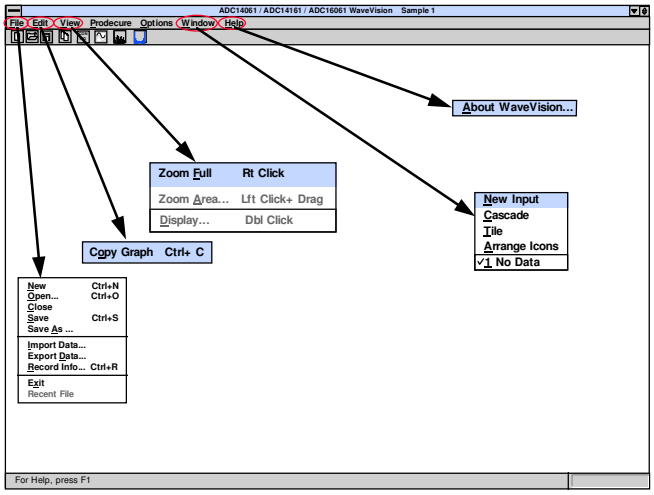
10.0 Evaluation Board Specifications

Board Size:	4.5" x 6.5" (11.4 x 16.5 cm)
Power Requirements:	+8V to +12V @ 100mA
Communications:	Parallel Port
Modes Supported:	Bi-Directional EPP & ECP
ADC Clock Frequency:	1.2MHz to 10MHz
Analog Input	
Nominal Voltage:	$2V_{P-P}$
Minimum Excursion:	1V
Maximum Excursion:	3V
Memory:	64k Words by 16 bits
Reference Voltage:	2.0V, nominal

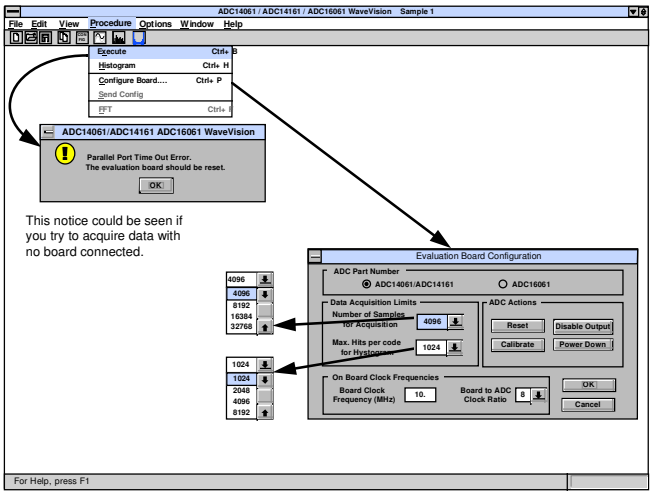
ADC14061
WaveVision Menu & Icon Description



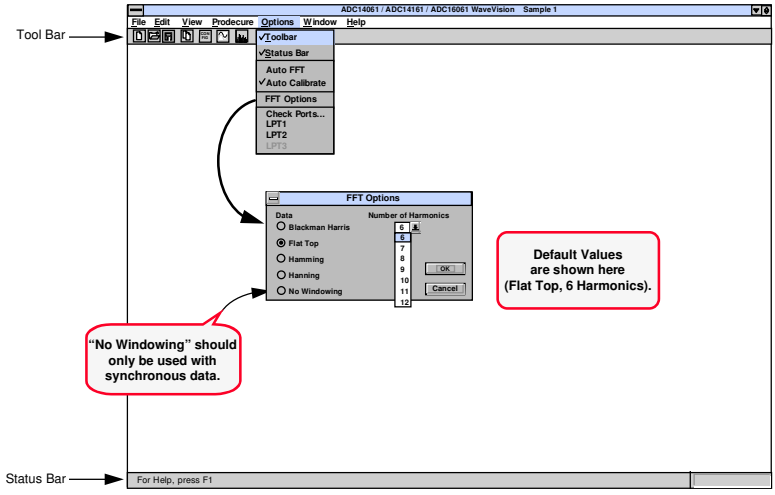
ADC14061
WaveVision Menu



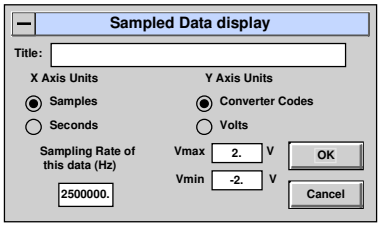
ADC14061
WaveVision Procedure Menu



ADC14061
WaveVision Options Menu

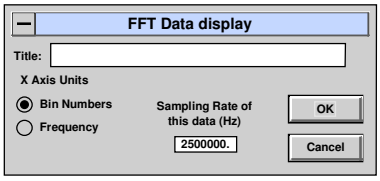


ADC14061
Sampled Data and FFT Data Display Options



This dialog box isobtained by double clicking on the sampled data plot.

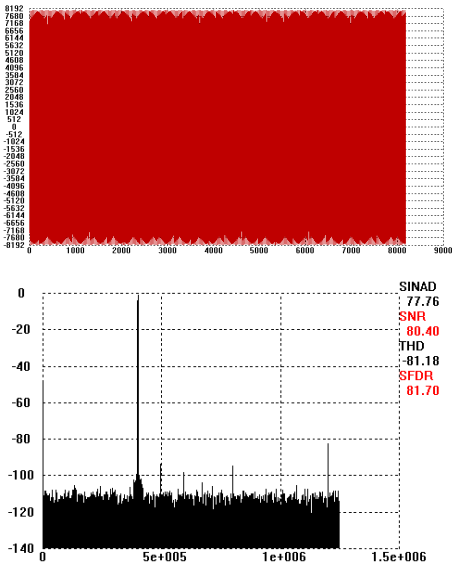
It allows you to set a title for the displayed waveform, to set X Axis and Y Axis units and to set min and max voltage levels.



This dialog box iis obtained by double clicking on the FFT plot.

It allows you to set a title for the FFT and to set X /Axis units.

ADC14061
WaveVision Data Display Examples



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